ARIVASANTH. M

Mobile: +91 9790841893
Mail: arivasanth@gmail.com

OBJECTIVE

Taking a challenging position in a multilingual environment to utilize my skills and abilities in the field of Teaching that offers professional growth while being resourceful, innovative and flexible.

EDUCATIONAL QUALIFICATION

- **M.E-Applied Electronics,(2008-2010)** **69.4%**
  Thiruvalluvar College of Engineering and Technology, Vandavasi.
  Anna University, Chennai.
- **B.E-Electronics and communication**, **(2004-2007)** **67.4%**
  Adhiyamaan Engineering College, Hosur
  Anna University, Chennai.
- **Diploma Electronics and communication, (2002-2004)** **90.91%**
  Dhanalakshmi Srinivasan Polytechnic College, Perambalur.
  Tamil Nadu Technical Board.
- **Higher Secondary Education**, **(2002)** **75.16%**
  Govt Higher Secondary School, Ponparappi.
- **S.S.L.C, (2000)** **86%**
  Govt Higher Secondary School, Ponparappi.

ACADEMIC EXPERIENCE as on May 2018: 8 Years and 10 Months

Name of the College	**Year of Experience 14 Year and 5 Months**	
	As Lecturer	**As Asst. Professor**
L.V.E.C, Kanchipuram	**1 Year**	**--**
Srinivasan Engineering College.Perambalur.	**1 Year**	**6 Year and 10 Months**
Meenakshi Ramaswamy Engieeing College, Thathanur	**--**	**Till Date 5 Year and 7 Months**

SUBJECTS HANDLED

- Digital Electronics.
- Digital Principles and System Design.
- Communication Theory.
- Digital Communication Techniques.
- Digital Communication.
- Basic Electrical and Electronics Engineering.
- Multimedia compression and communication.
- Electromagnetic Field and Theory.
- Electrical Drives and Controls.
- Medical Electronics.
- Electronic Circuits-I.
- Electronic Circuits-II.

- Measurements and Instrumentation.
- Embedded and Real Time Systems.
- Advance Digital System Design.(ME-VLSI)
- ASIC and FPGA Design. (ME-VLSI)
- Testing for VLSI Circuits. (ME-VLSI)

LABS HANDLED

- Digital Lab.
- Communication System Lab.
- Networks Lab.
- Electrical Machines Lab.
- Linear Integrated Circuits Lab.
- Engineering Practice Lab.
- Basic Electrical, Electronics & Instrumentation Lab.
- VLSI Design Lab II (M.E-VLSI)

SOFTWARE EXPOSURE

- Programming Languages: C, C++.
- Packages: MS Office, VHDL, Embedded C, MAT LAB, PSPICE.

AREA OF INTEREST

- Analog and Digital Communication.
- Digital Electronics.
- Medical Electronics

PROJECT PROFILE

- Data Security Using Context Switched Semaphore.(In M.E)
- Automated Multipurpose Industrial Security System Using Auto Dialer Tone And Voice Messaging.(In B.E)
- DTMF-Dual Tone Multi Frequency.(In Diploma)

PROJECTS GUIDED

- **TWELVE** UG projects were done under my guidance in VLSI, Embedded system domains.
- **FOUR** PG projects were done under my supervision in VLSI domain.

PROFESSIONAL EXPERIENCE

- Undergone In plant Training in BSNL, Trichirapalli.
- Undergone In plant Training in NLC, Neyveli.

PUBLICATIONS

International Conference: 3

- Presented a paper on "Optimized Design for Accumulator Based 3-Weight Pattern Generation", International Conference on Science, Engineering and Management-ICSEM"13 at Srinivasan Engineering College, Perambalur.
- Presented a paper on "Generation of Pseudo-Random Number Using WELL and Reseeding Method", International Conference on Competency Building Strategies in Business and Technology for Sustainable Development at Sri Ganesh School of Business Management, Salem.

- Presented a paper on "Optimization of Low Voltage Charge Pump with Stacking Power Gating Technique", International Conference on Electrical, Electronics & Computer Engineering-ICEECE 2015 at Vivekanandha College of Engineering for Women,Tiruchengode.

National conference: 2

- Presented a paper on "Data Security Using Context Switched Semaphore", National Conference on Recent Trends in communication Engineering at SASTRA University, Kumbakonam.
- Presented a paper on "Optimization of Low Voltage Charge Pump with Stacking Power Gating for Low Leakages in Circuits", National Conference on Recent Trends in Communication and Information Technologies at Indira Ganesan College of Engineering, Trichy.

Journals: 3

- Published a paper on "Optimized Design for Accumulator Based 3-Weight Pattern Generation", International Journal Of Engineering Research and Technology(IJERT), Vol. 1, No. 1, April 2013.
- Published a paper on "Generation of Pseudo-Random Number Using WELL and Reseeding Method", International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 4, Issue 3, March 2015.
- Published a paper on "Optimization of Low Voltage Charge Pump with Stacking Power Gating for Low Leakages in Circuits", International Journal of Engineering Research and Science & Technology-IJERST Vol.1, No.1, March 2015.

PERSONAL PROFILE

Name	:	Arivasanth.M.
Father Name	:	Mr.Muthukumarasamy. M.
Date of Birth	:	14.05.1985.
Gender	:	Male.
Marital Status	:	Married.
Languages Known	:	English &Tamil.
Permanent Address	:	1-258, North Street, Ponparappi Post, Ariyalur Dist-621710.

I hereby declared that the above information given is true to best of my knowledge and belief.

DATE:

PLACE: ARIVASANTH M